

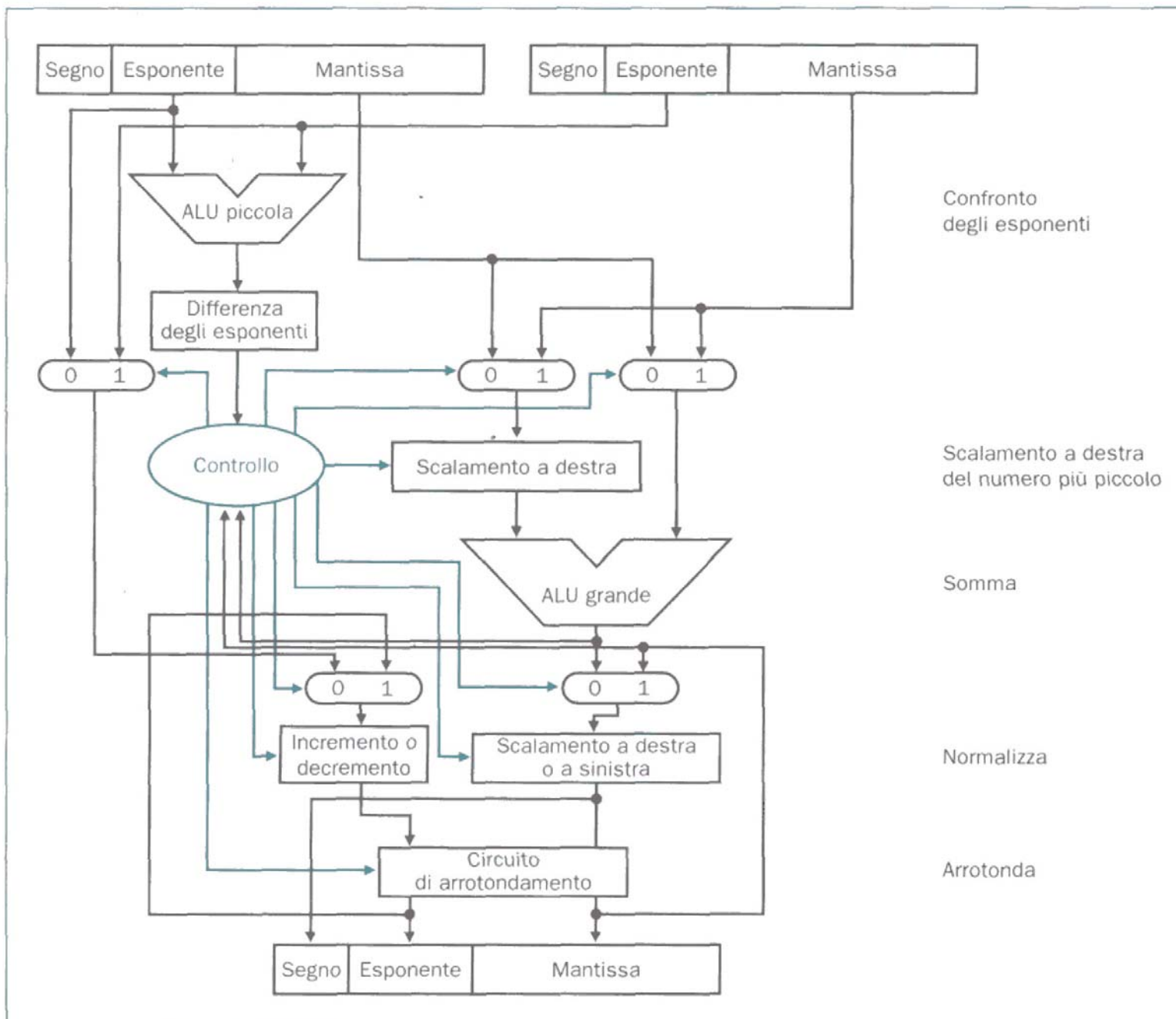
# L'architettura di riferimento degli elaboratori

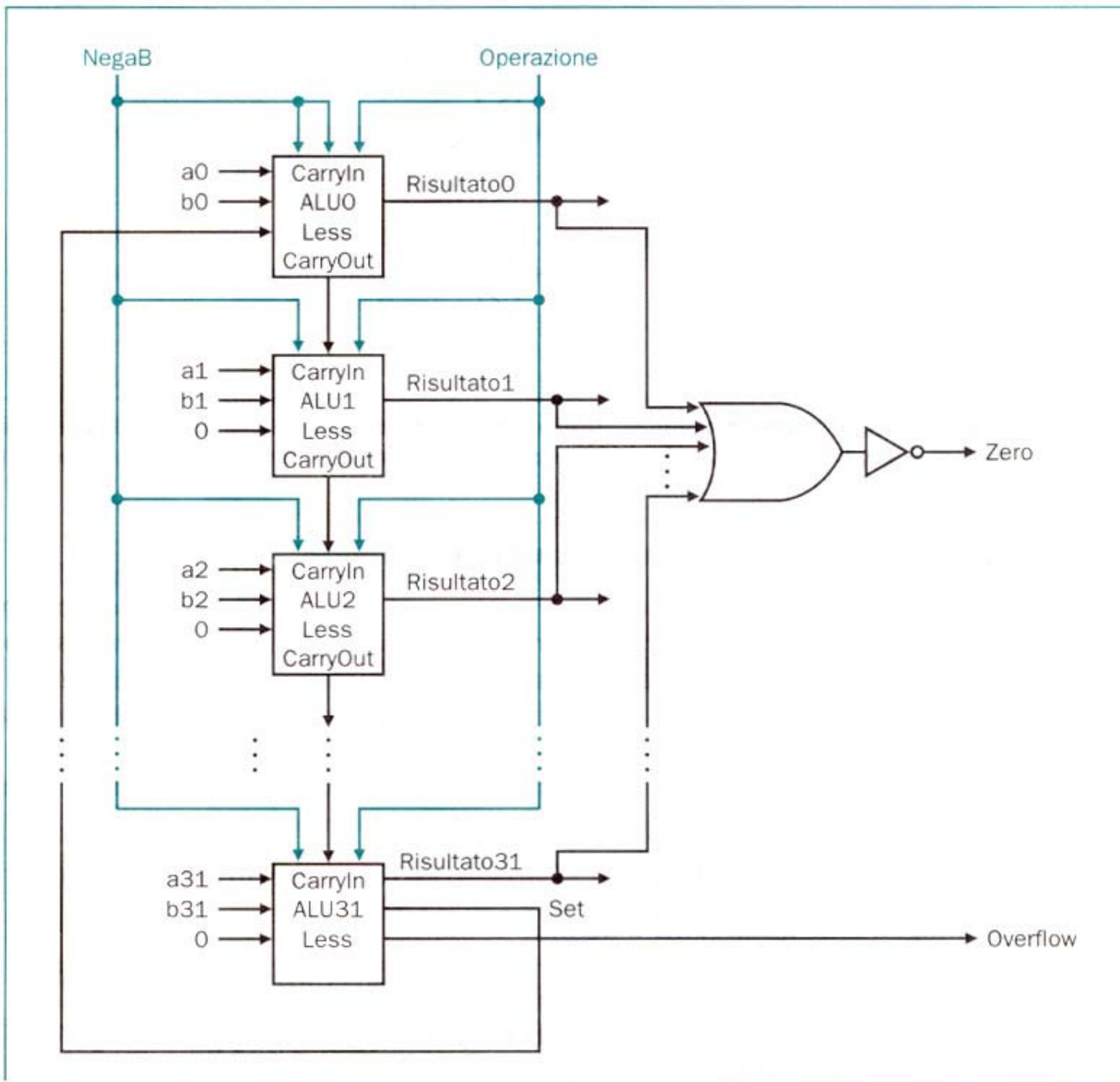
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## Architettura degli Elaboratori e delle Reti Turno I



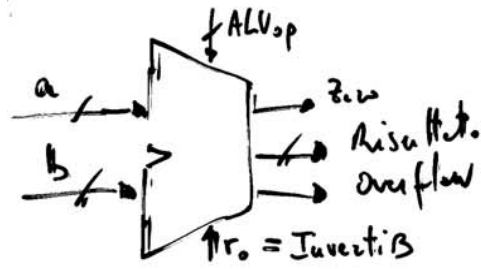
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# ALU - 1



1bit  $\downarrow$  Invert B

$x$ bit  $\downarrow$  ALUop

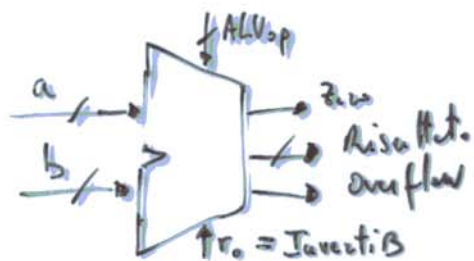
a 32bit  
b 32bit

32bit

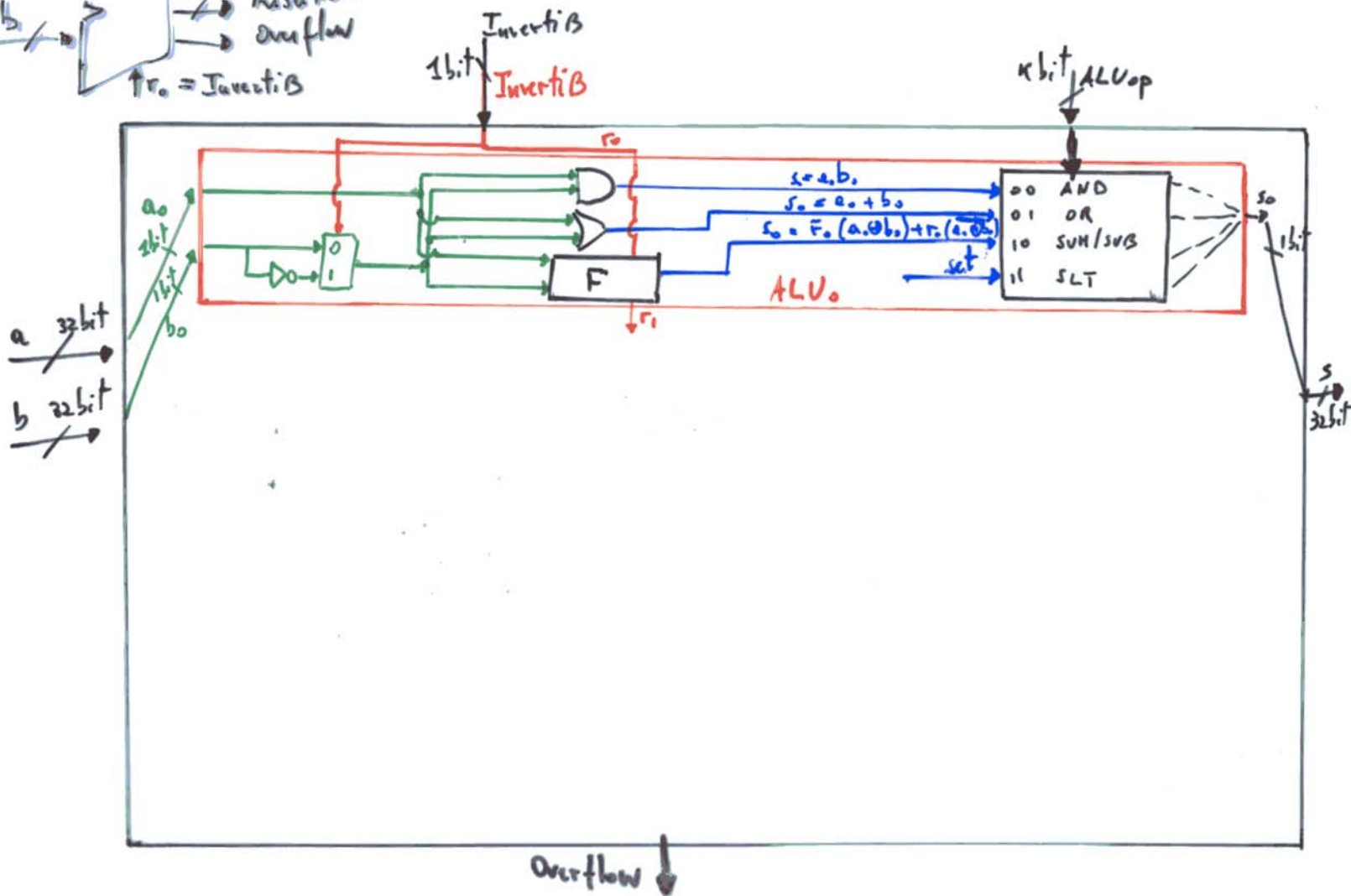
Overflow  $\downarrow$



# ALU - 2



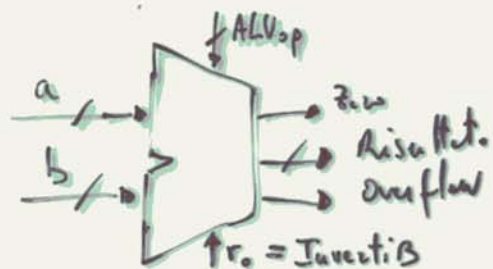
ZSTAD1: calcolo = selezione



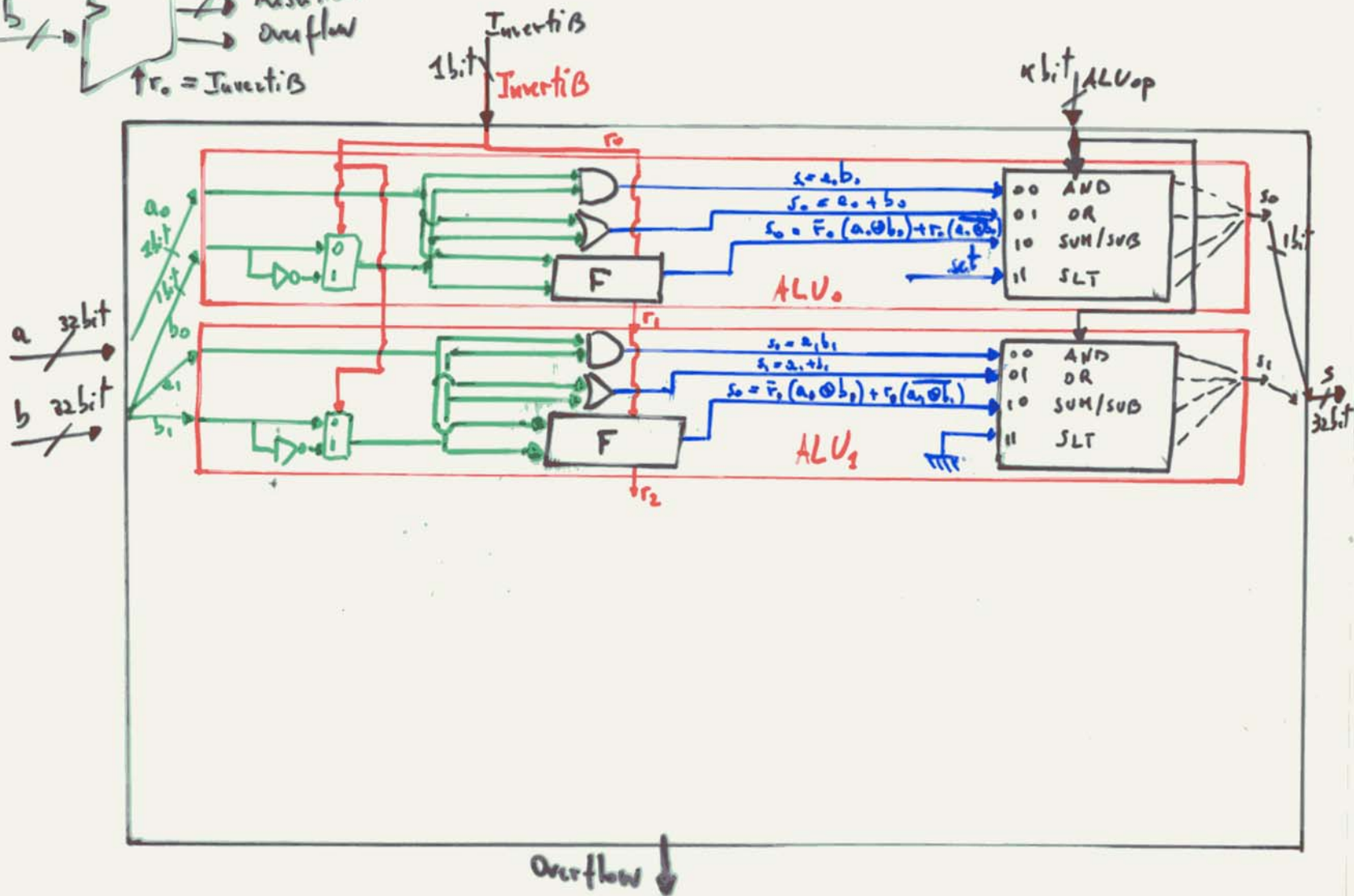
②  
① /



# ALU - 3



ZSTAD1: calcolo - selezione





# ALU - 4

